METHOD FOR MIN-CUT AND RATIO MIN-CUT PARTITIONING

Abstract of the Disclosure

The method of Edge-Node Interleave Sort for Leaching and Envelop (ENISLE) comprises mapping a circuit into a *V-E* plain to transform a circuit information into *V-E* plain. A plurality of sorting is performed for obtaining min-cut or/and ratio min-cut partitioning. The sorting includes (1) performing a first sorting step from an edge view based on a bottom side of the *V-E* plain; (2) performing a second sorting step from an node view based on a right side of the *V-E* plain; (3) performing a third sorting from said edge view based on a top side of the *V-E* plain; and (4) performing a fourth sorting step from said node view based on a left side of the *V-E* plain.